## REMARKS

Claims 1, 3, 4 and 11-17 are pending in the present application. Claims 1, 3 and 4 have been amended. Claims 11-17 have been presented herewith. Claims 2 and 5-10 have been canceled. Applicant reserves the right to file a divisional application including canceled claims 5-10.

## Priority Under 35 U.S.C. 119

Applicant notes the Examiner's acknowledgment of the Claim for Priority under 35 U.S.C. 119, and receipt of the certified copy of the Priority Document.

## Drawings

The drawings have been objected to as allegedly failing to comply with 37 C.F.R. 1.84(p)(5), because reference character 84 in Fig. 1 of the present application is not mentioned in the description. However, as described on page 10, lines 10-12 of the present application with respect to Fig. 1, NSG (non-doped silicate glass) **84** is disposed as a protective layer. Accordingly, since reference character 84 in Fig. 1 of the present application is described in the original application, the drawings are in compliance with 37 C.F.R. 1.84(p)(5). The Examiner is therefore respectfully requested to withdraw the objection to the drawings.

## Specification

The abstract of the disclosure has been objected to as including the word "comprises". The abstract has been corrected. The Examiner is therefore respectfully requested to withdraw this objection.

## Claim Rejections-35 U.S.C. 112

Claim 4 has been rejected under 35 U.S.C. 112, second paragraph. Claim 4 has been amended to feature "said source region", to improve antecedent basis. Applicant respectfully submits that claim 4 is in compliance with 35 U.S.C. 112, second paragraph, and thus respectfully urges the Examiner to withdraw this rejection.

## Claim Rejections-35 U.S.C. 102

Claims 1-4 have been rejected under 35 U.S.C. 102(e) as being anticipated by the Krishnan et al. reference (U.S. Patent No. 6,541,821). This rejection, insofar as it may pertain to the presently pending claims, is traversed for the following reasons.

The semiconductor device of claim 1 includes in combination a source region; a drain region; a body region; a gate region; and an extracting region "being in contact with both of said body region and said source region, said extracting region having a conductivity type which is the same as a conductivity type of said body region, and having an impurity concentration higher than that of said body region, wherein said extracting region extends from said source region to a position below the formed electrically conducting channel". Applicant respectfully submits that the Krishnan et al. reference as relied upon by the Examiner does not disclose these features.

As described beginning in column 2, line 29 of the Krishnan et al. reference with respect to Fig. 3, SOI transistor 100 includes two shallow $p^+$ pockets 114 each of p-type conductivity respectively adjacent the drain and source regions 110 and 112. The SOI transistor 100 further includes two deep $p^+$ pockets 116, each being of p-type conductivity and respectively adjacent to the drain and source regions 110 and 112. As specifically described in column 2, lines 61-65 of the Krishnan et al. reference, deep $p^+$ pockets 116 are doped so as to suppress punch-through current.

The Examiner has interpreted deep $p^+$ pockets 116 in Fig. 3 of the Krishnan et al. reference as the extracting region of claim 1. However, deep $p^+$ pockets 116 in Fig. 3 of the Krishnan et al. reference do not extend from a source region to a position below a formed electrically conducting channel, as would be necessary to meet the features of claim 1. That is, $p^+$ pockets 116 in Fig. 3 of the Krishnan et al. reference are formed at positions laterally away from channel 118. Accordingly, $p^+$ pocket regions 116 in Fig. 3 of the Krishnan et al. reference do not provide a structure which is capable of extracting remaining carriers in the body region by tunnel current, to thus suppress the occurrence of the substrate floating effect caused by the remaining carriers. This should be especially clear, because deep $p^+$ pockets 116 are specifically structured to suppress punch-through current. Applicant therefore respectfully submits that the semiconductor device of claim 1 distinguishes over the Krishnan et al. reference as relied upon by the Examiner, and that this rejection, insofar as it may pertain to claim 1, is improper for at least these reasons.

Claim 3 has been amended to be in independent form, and features in combination a defect layer "in which lattice defects are formed, said defect layer being formed in a neighborhood of said extracting region". Applicant respectfully submits that the Krishnan et al. reference as relied upon by the Examiner does not disclose these features.

The Examiner has interpreted shallow $p^+$ pockets 114 in Fig. 3 of the Krishnan et al. reference as the defect layer of claim 3. However, as described in column 2, lines 58-60 of the Krishnan et al. reference, shallow $p^+$ pockets 114 are p-type conductivity and are respectively adjacent to the drain and source regions. As further described in column 3, lines 11-13, deep $p^+$ pockets 114 may be doped with boron.

Accordingly, Applicant respectfully emphasizes that shallow $p^+$ pockets 114 in Fig. 3 of the Krishnan et al. reference are not specifically described as having lattice defects therein. Shallow $p^+$ pockets 114 in Fig. 3 of the Krishnan et al. reference therefore cannot be interpreted as the defect layer of claim 3. Applicant therefore respectfully submits that the semiconductor device of claim 3 distinguishes over the Krishnan et al. reference as relied upon by the Examiner, and that this rejection, insofar as it may pertain to claims 3 and 4, is improper for at least these reasons.

## Claims 11-17

Applicant respectfully submits that claims 11 and 12, as dependent upon claim 1, distinguish over and would not have obvious in view of the prior art as relied upon by the Examiner, for at least the reasons as set forth above with respect to claim 1, and by further reason of the features therein.

The semiconductor device of claim 13 includes in combination a semiconductor layer; a source region; a drain region; a body region; a gate and an extracting region "in said semiconductor layer, in contact with said body region and said source region, said extracting region having a conductivity type which is the same as a conductivity type of said body region, and having an impurity concentration higher than an impurity concentration of said body region, wherein said extracting region extends from said source region to directly under the gate".

As may be readily understood in Fig. 3 of the Krishnan et al. reference, deep $p^+$ pockets 116 are formed laterally away from gate 108, and thus are not formed directly under gate 108, as would be necessary to meet the features of claim 13. Applicant therefore respectfully submits that the semiconductor device of claims 13-17 distinguish over and would not have been obvious in view of the prior art as relied upon by the Examiner, for at least these reasons. Applicant also respectfully submits that the Krishnan et al. reference does not disclose a defect layer, as further featured in claims 16 and 17.

## Conclusion

The Examiner is respectfully requested to reconsider and withdraw the corresponding rejections, and to pass the claims of the present application to issue, for at least the above reasons.

In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (571) 283-0720 in the Washington, D.C. area, to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

VOLENTINE FRANCOS & WHITT, P.L.L.C.

Andrew J. Telesz, Jr.
Registration No. 33,581

One Freedom Square
11951 Freedom Drive, Suite 1260
Reston, Virginia 20190
Telephone No.: (571) 283-0270
Facsimile No.: (571) 283-0740